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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
TRAN, MICHAEL THANH

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,292	HOSOKAWA ET AL.	
	Examiner	Art Unit	
	Michael t. Tran	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,3,6,9,10,13 and 15-18* is/are allowed.

6)☒ Claim(s) *1,4,5,7,8,11,12,14,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

PRIMARY EXAMINER

DETAILED ACTION

1. In response to the Communications dated June 15, 2005, claims 1-20 are active in this application.

Claim Rejections – 35 U.S.C. § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1, 4, and 5 are rejected under 35 U.S.C 102(b) as being anticipated by Kubota [U.S. Patent #5,383,159].

With respect to claim 1, Kubota discloses a DRAM circuit comprising a plurality of aligned sense amplifiers [2, 4, 11, 13, 12, and 14 of figure 4], bit line pairs [BL1, /BL0, BL0, /BL1, etc. of figure 4] connected to the plurality of sense amplifiers [see figure 4],

respectively, and memory cells [within MB1-MB3 of figure 4] connected respectively to the bit lines constituting the bit line pairs, wherein the bit line pairs and the memory cells are alternately arranged on the right side and a left side of the sense amplifiers per N [N: natural number] aligned sense amplifiers [see figure 4].

With respect to claim 4, Kubota discloses the bit line pairs arranged on one of the right side and left side of the sense amplifier are both connected to corresponding data lines [word lines of figure 4] via bit switches.

With respect to figure 5, Kubota discloses the plurality of aligned sense amplifiers is divided every M sense amplifiers [M: natural number], and a set driver [see column 2] is disposed in a separated area.

4. Claim 7 is rejected under 35 U.S.C 102(b) as being anticipated by Kubota [U.S. Patent #5,383,159].

With respect to claim 7, Kubota discloses a DRAM circuit comprising: a plurality of sense amplifiers [2, 4, etc. of figure 4] arranged in Q lines each containing the P sense amplifiers; bit line pairs [BLO, /BLO, BL1, /BL1, etc. of figure 4] connected to the plurality of sense amplifiers, respectively; and memory cells [within MB1-MB3 of figure 4] connected respectively to the bit lines constituting the bit line pairs, wherein the bit line pairs and the memory cells are arranged every N [N: natural number] aligned sense amplifiers in the Q lines, alternately on a right side and a left side of the sense amplifiers, and P and Q are both integers of more than 3, and N is an arbitrary integer of more than 1 and less than [P/3] – it is noted that Kubota shows more than 1.

5. Claims 8, 11, and 12 are rejected under 35 U.S.C 102(b) as being anticipated by Kubota [U.S. Patent #5,383,159].

With respect to claim 8, Kubota discloses a DRAM circuit comprising a plurality of sense amplifiers SA [J,K] [2, 4, etc. of figure 4] arranged in Q lines each containing the P sense amplifiers, bit line pairs [BLO, /BLO, BL1, /BL1, etc. of figure 4] connected to the plurality of sense amplifiers SA, respectively, and memory cells [within MB1-MB3 of figure 4] connected respectively to the bit lines constituting the bit line pairs, wherein the sense amplifier SA [J,K] is connected to each of the bit line pairs arranged between the sense amplifier SA [J,K] and a sense amplifier SA [J, K-1] [2, 4, etc. of figure 4] in one next line; a sense amplifier SA [J+1,K] [2, 4, etc. of figure 4] is connected to the bit line pairs arranged between the sense amplifier SA [J+1,K] and sense amplifier SA [J+1, K+1] [2, 4, etc. of figure 4] in another next line; a sense amplifier SA [J+2, K] [2, 4, etc. of figure 4] is connected to each of the bit line pairs arranged between the sense amplifier SA [J+2, K] and a sense amplifier SA [J+2, K-1] [2, 4, etc. of figure 4] in one next line; and P and Q are both integers of more than 3, J is an arbitrary integer of more than 1 and less than P, and K is an arbitrary integer of more than 1 and less than Q.

With respect to claim 11, Kubota discloses the bit line pairs arranged in one space between the sense amplifier SA [J,K] and the sense amplifier SA [J,K-1] in the next line are both connected to corresponding data lines [word lines of figure 4] via bit switches.

With respect to claim 12, Kubota discloses the plurality of sense amplifiers, whose number arranged in on line is P, is divided every M sense amplifiers [M: natural number], and a set driver [see column 2] is disposed in a separated area.

6. Claim 14 is rejected under 35 U.S.C 102(b) as being anticipated by Kubota [U.S. Patent #5,383,159].

With respect to claim 14, Kubota discloses a DRAM circuit comprising: a plurality of sense amplifiers SA [J,K] [2,4, etc. of figure 4] arranged in Q lines each containing the P sense amplifiers; bit line pairs [BL0, /BL0, BL1, /BL1, etc. of figure 4] connected to the plurality of sense amplifiers SA [J,K], respectively; and memory cells [within MB1-MB3 of figure 4] connected respectively to the bit lines constituting the bit line pairs, wherein the sense amplifier SA [J,K] and a sense amplifier SA [J+1,K] [[2,4, etc. of figure 4] are each connected to each of the bit line pairs arranged between a sense amplifier SA [J, K-1] [2,4, etc. of figure 4] in one next line and a sense amplifier SA [J+1, K-1] [2,4, etc. of figure 4]; a sense amplifier SA [J+2, K] [2,4, etc. of figure 4] and a sense amplifier SA [J+3,K] [2,4, etc. of figure 4] are each connected to the bit line pairs arranged between a sense amplifier SA [J+2,K+1] [2,4, etc. of figure 4] in another next line and a sense amplifier SA [J+3, K+1] [2,4, etc. of figure 4]; a sense amplifier SA [J+4, K] [2,4, etc. of figure 4] and a sense amplifier SA [J+5, K] [2,4, etc. of figure 4] are each connected to each of the bit line pairs arranged between a sense amplifier SA [J+4, K-1] [2,4, etc. of figure 4] in one next line and a sense amplifier SA [J+5, K-1] [2,4, etc. of figure 4]; and P and Q are both integers of more than 6, J is an arbitrary integer

of more than 1 and less than P, and K is an arbitrary integer of more than 1 and less than Q. It is noted that Kubota discloses, in figure 4, a configuration that can be interpreted as having a greater number of sense amplifiers and bit line pairs than shown.

7. Claim 19 is rejected under 35 U.S.C 102(b) as being anticipated by Kubota [U.S. Patent #5,383,159].

With respect to claim 19, Kubota discloses a DRAM circuit comprising a plurality of aligned sense amplifiers [2, 4, etc. of figure 4], bit line pairs [BL0, /BL0, BL1, /BL1, etc. of figure 4] connected to the plurality of sense amplifiers, respectively, and memory cells [within MB1-MB3 of figure 4] connected respectively to the bit lines constituting the bit line pairs, wherein the bit line pairs and the memory cells are alternately arranged on a right side and a left side of the sense amplifiers per N [N: natural number] aligned sense amplifiers so that first bit line pairs and memory cells are arranged on a right side of a first sense amplifier, a second bit line pairs and memory cells are arranged on a left side of a second sense amplifier, third bit line pairs and memory cells are arranged on a right side of a third sense amplifier, and so on until all bit line pairs and memory cells have been alternately arranged per the N aligned sense amplifiers – see figure 4.

8. Claim 20 is rejected under 35 U.S.C 102(b) as being anticipated by Kubota [U.S. Patent #5,383,159].

With respect to claim 20, Kubota discloses a DRAM circuit comprising: a plurality of sense amplifiers [2,4, etc. of figure 4] arranged in Q lines each containing the P sense amplifiers; bit line pairs [BL0, /BL0, BL1, /BL1, etc. of figure 4] connected to the plurality of sense amplifiers, respectively, and memory cells [within MB1-MB3 of figure 4] connected respectively to the bit lines constituting the bit line pairs, wherein the bit line pairs and the memory cells are arranged every N [N: natural number] aligned sense amplifiers in the Q lines, alternately on a right side and a left side of the sense amplifiers, and P and Q are both integers of more than 3, and memory cells are arranged on a right side of a first sense amplifier in a first line, second bit line pairs and memory cells are arranged on a left side of a second sense amplifier in a first line, third bit line pairs and memory cells are arranged on a right side of a third sense amplifier in a first line, and so on until all bit line pairs and memory cells have been alternately arranged per the N aligned sense amplifiers in the Q lines – see figure 4.

Allowable Subject Matter

9. Claims 2, 3, 6, 9, 10, 13, and 15-18 are allowable over the prior art of record.

10. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- Wherein, further, two bit lines constituting the bit line pair, which is arranged in a space opposite to the one space between the sense amplifier SA [J,K] and the

sense amplifier SA [J, K+1] or SA [J, K-1] in the next line, do not cross, and a space therebetween widens or narrows on the way.

- A step of activating the plurality of sense amplifiers connected to the bit line pairs and memory cells arranged on the right side [upper side] of the sense amplifiers, and the plurality of sense amplifiers connected to the bit line pairs and memory cells arranged on the left side [lower side] of the sense amplifiers at different timing, when data is read.

Remarks

11. Applicant's arguments filed June 15, 2005 have been fully considered but they are not persuasive.

Applicant argued that the Kubota reference does not disclose a memory structure comprising a plurality of sense amplifiers arranged adjacent to each other having only one pair of bit lines connected to each of them. Applicant further pointed out that the disclosure of figure 5 clearly points out that particular limitation. Additionally, Applicant requested that since the disclosure points out that limitation, figures 5 and 7 should be amended to include that structure. However, after reviewing the cited portion of the disclosure for figure 5 that the Applicant referred to in the remarks, the Examiner does not find the stated limitation. According to the cited portion, the disclosure states that there exists "bit line pairs to be connected are alternately interchanged". The Examiner does not see how this statement can limit an interpretation to just "only one" pair of bit lines. Further, it appears that the requested drawing amendment is new matter and will

not be entered. Furthermore, it is noted that the disclosure can not be amended to overcome the applied reference.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

Conclusion

12. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

14. Any inquiry of a general nature or relating to the status of this application

should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
July 29, 2005

MICHAEL T. TRAN
PRIMARY EXAMINER